

100397 U.S. PTO
10/003048
12/06/01

PATENT NUMBER and
ISSUE DATE

U.S. UTILITY Patent Application

APPLICATION NO. 10/003048	CONT/PRIOR F	CLASS 326	SUBCLASS 86	ART UNIT 2819	EXAMINER V. TAN
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APPL. NUM 10000048	FILING DATE 12/06/2001	CLASS 326	SUBCLASS	GA1 2819	EXAMINER
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**APPLICANTS: Matsuzaki Yasuou;

**CONTINUING DATA VERIFIED:

None

** FOREIGN APPLICATIONS VERIFIED:

JAPAN 2001-219519 07/19/2001

ok

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PG. PUB. DO NOT PUBLISH <input type="checkbox"/>	RESCIND <input type="checkbox"/>
Foreign priority claimed <input type="checkbox"/> yes <input type="checkbox"/> no	ATTORNEY DOCKET NO
35 USC 119 conditions met <input type="checkbox"/> yes <input type="checkbox"/> no	108397-00052
Verified and Acknowledged: examiner's initials	
TITLE: Input/output interface and semiconductor integrated circuit having input/output interface	

U.S. DEPT. OF COM./PAT. & TM-PTO-436L (Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		Total Claims	Print Claim for O.G.
Assistant Examiner		DRAWING	
ISSUE FEE		Sheets Drawg.	Figs. Drawg.
Amount Due	Date Paid	Print Fig.	
Primary Examiner		Application Examiner	
PREPARED FOR ISSUE			
<input type="checkbox"/> TERMINAL DISCLAIMER		WARNING: The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code Title 35, Sections 122, 181 and 368, Possession outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.	

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